Gustavo Andrés Ramirez Lopez

Software Engineer

EMAIL garamirezl@outlook.com   **PHONE** +57 301 4477647

LOCATION Bogotá D.C

PORTFOLIO https://areshkew.github.io/portfolio/

STATEMENT

I'm a full-stack software engineer with experience in front-end development, backend, and database optimization. I focus on improving the speed and functionality of web applications and enjoy learning new tools and technologies to solve problems and enhance user experiences.

LINKS

LinkedIn
https://www.linkedin.com/in/areshk/

GitHub
https://github.com/Areshkew

EDUCATION

UTP Universidad Tecnológica de Pereira
Graduated in June 2025

Bachelor's Degree Computer Systems Engineering

SENA
Graduated in November 2019

Software Development Technician

SKILLS

Web Development

HTML/CSS/JS · Angular · Typescript · Node.js · MongoDB · PostgreSQL · C/C++ · FastApi · Python · TailwindCSS · Bun

Industry Knowledge

Api Design · Perfomance Optimization · Cloud Infrastructure · DevOps · DB design

Tools

Excel · PostMan · Docker · Azure · Git · Github · Github Actions (CI/CD) · Selenium · PgAdmin · Jira

CERTIFICATIONS

LinkedIn
September 2024
Scrum: Advanced

Coursera
June 2023
Containers w/ Docker, Kubernetes & OpenShift

Código Facilito
May 2023
NGinx

Código Facilito
May 2023
noSQL - MongoDB

OpenBootcamp
November 2022
Angular

SENA
June 2017
Teamwork and Assertive Communication

LANGUAGES

Spanish
Native

English
B2

WORK EXPERIENCE

AI and Neuroscience Researcher at SNEIA • UTP
Aug 2024 → Current   Pereira, Risaralda (Part Time)

- Worked on the development and training of artificial intelligence models, specifically in Natural Language Processing using NLP.js with a focus on text classification and trained a model using a dataset of 15,000 records, reducing prediction error to 11%, significantly improving accuracy in classifying new data.
- Conducted research and data analysis to optimize the efficiency and accuracy of trained models.

Frontend Engineer • Konceptual
Apr 2021 → Mar 2022   Bogotá D.C (remote)

- Collaborated with a team to add new features to a POS system, ensuring compliance with DIAN regulations in Colombia.
- Optimized websites for performance and user experience, improving load times and responsiveness.
- Converted design mock-ups into functional and responsive interfaces using Angular.
- Managed code versioning and changes with Git, ensuring smooth development workflows.
- Ensured functionality and resolved issues through debugging and testing.

Freelance Frontend Developer
Aug 2020 → Feb 2021   Bogotá D.C (Remote)

- Developed a full CRUD system for product and availability management using Angular for the frontend and Node.js with Express for the backend.
- Implemented features to manage cities, quoters, factors, lines, and prices, improving operational efficiency.
- Built secure user authentication using tokens to enhance the system's security.

PROJECTS

LibHub • UTP
Feb 2023 → Jul 2023   Pereira, Risaralda

Developed using Python (FastAPI), Angular (TypeScript), CI/CD (GitHub Actions), Web Scraping (Python), Bulk Data Upload, and PostgreSQL.

- Implemented web scraping script using Python to extract a significant amount of books.
- Designed and optimized a bulk data upload system, allowing efficient import of large datasets into the database using temporary tables and COPY in PostgreSQL.
- Deployed the application on Oracle Cloud VPS through GitHub Actions (CI/CD) triggered by merges to the main branch, ensuring scalability and reliability, while configuring Nginx for load balancing and serving the application.
- Participated in the software design process, gathering requirements, creating user stories, and developing UML diagrams to ensure a clear and structured development process that aligns with business objectives.

RISC-V • UTP
Aug 2023 → Nov 2023   Pereira, Risaralda

Developed a complete project focused on RISC-V architecture, including a C++ compiler, a Python-based assembler, and a Verilog implementation of both single-cycle and pipelined RISC-V processors.

- Enhanced processor performance by implementing pipelining techniques in Verilog, reducing instruction latency and improving throughput.
- Implemented hazard detection and forwarding mechanisms to optimize the pipelined processor, minimizing stalls and improving execution flow.
- Applied deep knowledge of hardware-software interaction, handling direct memory access, register manipulation, and instruction cycle control.
- Built a memory visualizer using Python and Tkinter to simulate and visualize memory operations during processor testing, aiding in debugging and enhancing understanding of memory behavior.